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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/043,474 | 01/10/2002 | Leonid Baraz | 42390.P8254 | 6444 |

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

| EXAMINER | |
|---|---|
| CHOW, CHIH CHING | |
| **ART UNIT** | **PAPER NUMBER** |
| 2122 | |

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/043,474 | BARAZ ET AL. | |
| | Examiner | Art Unit | |
| | Chih-Ching Chow | 2122 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is responsive to the application filed on January 10, 2002.

2. The priority date considered for this application is January 10, 2002.

3. Claims 1-27 have been examined.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4-6, 9-11, 13-15, 18-20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US2003/0079210, by Peter Markstein et al. (hereinafter "Markstein"), in view of 'An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies', International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy Norris and Lori L. Pollock. (hereinafter "Pollock").

| CLAIM | Markstein / Pollock |
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| 1. A machine-implemented method comprising:<br>analyzing one or more instructions of a program; and<br>modifying the program to expand a register set for a routine in the program. | Markstein teaches the feature of analyzing a program, in Markstein, paragraph 48, "the entire **source code is analyzed** to generate a control flow graph" (*analyzing instructions of a program*) ; Markstein also teaches 'expand a register set', in paragraph 6, last two sentences, "A prologue and epilog typically includes code executed before and after a **subroutine** or **program**. For example, when a prologue is executed stack space may be allocated for **saving necessary context**, such as **saving callee-saved registers**. When an epilog is executed, the compiler may **restore any necessary registers**."; in paragraph 51, "**Additional register allocation** may be needed if a single intermediate level instruction expands into more than one target level instruction". Markstein teaches all aspects of claim 1, but he does not mention 'modifying program' specifically, however, Pollock teaches it in an analogous prior art. In Pollock's page 169, under '1. Introduction', second sentence, "A scheduler that **rearranges code within a basic block** (a *routine in the program*) in isolation of the rest of the program is called a local scheduler; a scheduler that **moves instructions across basic blocks** by considering the effects of code movement on a global level is called a global scheduler" (*modifying the program*). |

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| | It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Markstein's disclosure of the analyzing program and expanding registers by modifying program taught by Pollock, for the purpose of optimizing compilers for supporting instruction level parallelism (Pollock page 169, under 'Introduction', first sentence). |
| 2. The method of claim 1, comprising:<br>identifying one or more register moves for the expanded register set; and<br>modifying the program to perform the identified one or more register moves. | For the feature of claim 1 see claim 1 rejection. In Markstein paragraph 9, "**identifying** an operand from the intermediate code to store in a real **register**; and selecting an appropriate class of real registers to **store the operand**." See claim rejection 1 has for 'modifying program' feature. |
| 4. The method of claim 1, wherein the modifying the program comprises modifying the program to expand a register set for a callee routine of the program. | For the feature of claim 1 see claim 1 rejection. Again, in Markstein paragraph 51, "**Additional register allocation may be needed** if a single intermediate level instruction expands into more than one target level instruction", the additional register (*expand register set*) can be for a **callee** routine or a **caller** routine. See Markstein, paragraph 27, "Different classes of real registers may include **caller-saved registers** and **callee-saved registers. Callee-saved registers** are preferably used to store local variables and stack items", also in the same paragraph, "A program may be compiled such that a library **routine** may store a temporary computation in a |

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| | **caller-saved register**. Local variables and stack items, which are generally needed for a longer period of time, are stored in **callee-saved registers** (*for a callee routine of the program*)". |
| 5. The method of claim 4, comprising: modifying the program to expand a register set for a caller routine that is to call the callee routine. | For the feature of claim 4 see claim 4 rejection. In Markstein's disclosure cited in claim 4 rejection, it covers both callee routine and caller routine, and the caller routine can call the callee routine. |
| 6. The method of claim 5, wherein the modifying the program to expand a register set for the callee routine comprises modifying the program to expand a register set that includes one or more registers of the register set for the caller routine. | For the feature of claim 5 see claim 5 rejection. For the rest of the claim 6 feature see claim 4 rejection. |
| 9. The method of claim 1, comprising: modifying the program to store and/or use data in one or more registers added to the register set to help analyze execution of the program. | See claim 1 rejection. |
| 10. A machine-readable medium having instructions that, if executed by a machine, cause the machine to perform a method comprising:<br>analyzing one or more instructions of a program; and<br>modifying the program to expand a register set for a routine in the program. | Markstein's FIG. 4 shows a 'machine-readable' medium as cited in claim 10. For the rest of the features see claim 1 rejection. |

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| 11. The machine-readable medium of claim 10, wherein the method comprises:<br>identifying one or more register moves for the expanded register set; and<br>modifying the program to perform the identified one or more register moves. | For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 2 rejection. |
| 13. The machine-readable medium of claim 10, wherein the modifying the program comprises modifying the program to expand a register set for a callee routine of the program. | For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 4 rejection. |
| 14. The machine-readable medium of claim 13, wherein the method comprises: modifying the program to expand a register set for a caller routine that is to call the callee routine. | For the feature of claim 13 see claim 13 rejection. For the rest of the features see claim 5 rejection. |
| 15. The machine-readable medium of claim 14, wherein the modifying the program to expand a register set for the callee routine comprises modifying the program to expand a register set that includes one or more registers of the register set for the caller routine. | For the feature of claim 14 see claim 14 rejection. For the rest of the features see claim 6 rejection. |
| 18. The machine-readable medium of claim 10, wherein the method comprises: modifying the program to store and/or use data in one or more registers added to the register set to help analyze execution of the program. | For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 9 rejection. |
| 19. A system comprising:<br>a processor to execute instructions; | Same as claim 10 rejection. |

and
a medium having instructions to analyze one or more instructions of a program and to modify the program to expand a register set for a routine in the program.

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| 20. The system of claim 19, the medium having instructions to identify one or more register moves for the expanded register set and to modify the program to perform the identified one or more register moves. | For the feature of claim 19 see claim 19 rejection. For the rest of the features see claim 2 rejection. |
| 22. The system of claim 19, the medium having instructions to modify the program to expand a register set for a callee routine of the program. | For the feature of claim 19 see claim 19 rejection. For the rest of the features see claim 4 rejection. |
| 23. The system of claim 22, the medium having instructions to modify the program to expand a register set for a caller routine that is to call the callee routine. | For the feature of claim 22 see claim 22 rejection. For the rest of the features see claim 5 rejection. |
| 24. The system of claim 23, the medium having instructions to modify the program to expand a register set that includes one or more registers of the register set for the caller routine. | For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 6 rejection. |

6. Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US2003/0079210, by Peter Markstein et al. (hereinafter "Markstein"), in view of 'An Experimental Study of Several Cooperative Register

Allocation and Instruction Scheduling Strategies', International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy Norris and Lori L. Pollock. (hereinafter "Pollock"), and further in view of U.S. Patent No. 5, 644,709 by Todd Michael Austin (hereinafter "Austin").

| CLAIM | Markstein / Pollock / Austin |
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| 3. The method of claim 2, wherein the identifying comprises:<br>(a) defining one or more move chains for the expanded register set, and<br>(b) identifying a sequence of one or more register moves based on the defined one or more move chains. | For the feature of claim 2 see claim 2 rejection. In Pollock page 169, under 'Introduction', "Register allocation techniques are either local, global, or interprocedural depending on whether the allocator attempts an **assignment of registers** to values within **basic blocks** (*chain*) in isolation of other **basic blocks**, across **basic blocks** of a procedure, or across procedure boundaries, respectively." The 'identifying register' feature is the 'register allocation' recited in Pollock's prior art, see claim rejection 1. Pollock teaches register allocation of claim 3, but he does not mention 'move chain' specifically, however, Austin teaches it in an analogous prior art. In Austin column 7, lines 19-26, "A **call-chain** is the state of the stack at some point in a program's execution; it is composed of **a sequence of function names**; functions higher in the **call-chain** call (possibly indirectly) the functions lower in the call **chain**; neighbors in the **call-chain** share a |

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| | direct **caller-callee relationship**. A partial **call-chain** is a subset of the current complete call-chain, usually taken from the bottom of the complete call chain; partial call-chains are usually employed to reduce storage requirements."<br>It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Markstein's and Pollock's disclosures of the analyzing program and expanding registers by call chain taught by Austin, for the purpose of adjusting the appropriate counts at calls (Austin column 7, lines 34-35) thus no callee routine would be left out during a program rearrangement. |
| 12. The machine-readable medium of claim 11, wherein the identifying comprises:<br>(a) defining one or more move chains for the expanded register set, and<br>(b) identifying a sequence of one or more register moves based on the defined one or more move chains. | For the feature of claim 11 see claim 11 rejection. For the rest of the features see claim 3 rejection. |
| 21. The system of claim 20, the medium having instructions to define one or more move chains for the expanded register set and to identify a sequence of one or more register moves based on the defined one or more move chains. | For the feature of claim 20 see claim 20 rejection. For the rest of the features see claim 3 rejection. |

7. Claims 7, 8, 16, 17, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US2003/0079210, by Peter Markstein et al. (hereinafter "Markstein"), in view of 'An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies', International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy Norris and Lori L. Pollock. (hereinafter "Pollock"), and further in view of U.S. Patent No. 6,256, 777 by William B. Ackerman (hereinafter "Ackerman").

| CLAIM | Markstein / Pollock / Ackerman |
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| 7. The method of claim 5, comprising:<br>(a) identifying one or more register moves for the register set of the caller routine; and<br>(b) modifying the program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine. | For the feature of claim 5 see claim 5 rejection. Markstein and Pollock teach program analysis and register allocation of claim 5, but he does not mention 'modifying the program' specifically, however, Ackerman teaches it in an analogous prior art. In Ackerman, column 2, lines 40-44, "information that identifies changes of variable value **assignments to registers** at plural steps of program. The information further includes data that identifies any **change of sequence of machine code** instructions from the sequence of source code statements that gave rise to the machine code instructions."<br>It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement |

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| | Markstein's and Pollock's disclosures of the analyzing program and expanding registers by changing the program sequence taught by Ackerman, for the purpose of rendering the machine code into a more efficiently executing program. (Ackerman column 1, lines 30-31). |
| 8. The method of claim 5, comprising:<br>(a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and<br>(b) modifying the program to perform the identified register move. | For the feature of claim 5 see claim 5 rejection. For the rest of the feature in claim 8 see claim 7 rejection. |
| 16. The machine-readable medium of claim 14, wherein the method comprises:<br>(a) identifying one or more register moves for the register set of the caller routine; and<br>(b) modifying the program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine. | For the feature of claim 14 see claim 14 rejection. For the rest of the features see claim 7 rejection. |
| 17. The machine-readable medium of claim 14, wherein the method comprises:<br>(a) identifying a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine; and<br>(b) modifying the program to perform | For the feature of claim 14 see claim 14 rejection. For the rest of the features see claim 8 rejection. |

the identified register move.

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| 25. The system of claim 23, the medium having instructions to identify one or more register moves for the register set of the caller routine and to modify the program to perform the identified one or more register moves prior to or upon returning from the callee routine to the caller routine. | For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 7 rejection. |
| 26. The system of claim 23, the medium having instructions to identify a register move from a register added to the register set for the caller routine to a register added to the register set for the callee routine and to modify the program to perform the identified register move. | For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 8 rejection. |
| 27. The system of claim 19, the medium having instructions to modify the program to store and/or use data in one or more registers added to the register set to help analyze execution of the program. | For the feature of claim 19 see claim 19 rejection. For the rest of the features see claim 9 rejection. |

## *Conclusion*

The following summarizes the status of the claims:

35 USC § 103 claim rejection: 1-27.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow
Examiner
Art Unit 2122

CC

Hoanginh Antony Nguyen Ba

ANTONY NGUYEN-BA
PRIMARY EXAMINER